

Form 1449*	Atty. Docket No.: 884.400US1	Serial No. <u>Unknown</u> 09/873557
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Amaresh Pangal et al.	
	Filing Date: Herewith	Group: <u>Unknown</u>

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	5,764,089	06/09/1998	Partovi, H., et al.	327	200	08/30/96
	5,898,330	04/27/1999	Klass, E.F.	327	210	06/03/97
	5,900,759	05/04/1999	Tam, K.W.	327	201	06/26/97

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**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
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(Including Author, Title, Date, Pertinent Pages, Etc.)

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ch	Beaumont-Smith, A., et al., "Reduced Latency IEEE Floating-Point Standard Adder Architectures", <u>Proceedings of the 14th IEEE Symposium on Computer Arithmetic</u> , 8 pgs., (1998)
CD	Even, G., et al., "On the Design of IEEE Compliant Floating Point Units", <u>IEEE Transactions on Computers</u> , Vol. 49, 398-413, (May 2000)
CD	Goto, G., et al., "A 54 X 54-b Regularly Structured Tree Multiplier", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 27, 1229-1236, (Sept. 1992)
CD	Ide, N., et al., "2.44-GFLOPS 300-MHz Floating-Point Vector-Processing Unit for High-Performance 3-D Graphics Computing", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 35, 1025-1033, (July 2000)
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CD	Lee, K.T., et al., "1 GHz Leading Zero Anticipator Using Independent Sign-Bit Determination Logic", <u>2000 Symposium on VLSI Circuits Digest of Technical Papers</u> , 194-195, (2000)
CD	Partovi, H., et al., "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements", <u>Proceedings of the IEEE International Solid-State Circuits Conference, Digest of Technical Papers and Slide Supplement</u> , NexGen Inc., Milpitas, CA, 40 pgs., (1996)

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*Substitute Disclosure Statement Form (PTO-1449)

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Sheet 1 of 1

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OP	Hokenek, E., et al., "Second-Generation RISC Floating Point with Multiply - Add Fused", <u>IEEE Journal of Solid-State Circuits</u> , 25 (5), pp. 1207-1213, (1990)
CP	Luo, Z., et al., "Accelerating Pipelined Integer and Floating-Point Accumulations in Configurable Hardware with Delayed Addition Techniques", <u>IEEE Transactions on Computers</u> , 49 (3), 208-218, (March 2000)
CD	Panneerselvam, G., et al., "Multiply-Add Fused RISC Architectures for DSP Applications", <u>IEEE Pac Rim</u> , pp. 108-111, (1993)

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